Comparison Between Quadruple-Sampled State-Variable-Derivative Deadbeat Current Controller with PI Current Controller in Grid-Connected Inverter

Garba Elhassan*,**, Shamsul Aizam Zulkifli*, Solomon Zakwoi Iliya**,***, Zainab Yunusa ****, Mohammed Ahmed*****, Mubashir Hayat Khan*, Ronald Jackson*, Nadia Zeb*

*Faculty of Electrical and Electronics Engineering, Universiti Tun Hussein Onn, 86400 Malaysia.

**National Space Research and Development Agency, Obasanjo Space Centre, Umar Musa Yar'adua way, PMB 437, Lugbe, Abuja, Nigeria.

***Institute of Space Science and Engineering, African University of Science and Technology, Umaru Musa Yar'adua Way, Galadimawa 900109, Abuja, Nigeria.

**** Department of Electrical Engineering, University of Hafr Al Batin ,39524, Saudi Arabia.

*****Department of Electrical Engineering, Abubakar Tafawa Balewa University, Tafawa Balewa Way PMB 0248, Bauchi State, Nigeria.

(ge180033@siswa.uthm.edu.my, aizam@uthm.edu.my, iliya@isse.edu.ng, zainaby@uhb.edu.sa, amohammed3@atbu.edu.ng, ge180116@siswa.uthm.edu.my, he180095@siswa.uthm.edu.my, nadia.zeb@gmail.com)

‡ Corresponding Authors: Garba Elhassan, Tel:+60149861815,ge180033@siswa.uthm.edu.my and Shamsul Aizam Zulkifli, UTHM, Johor, 86400 Malaysia Tel: +60 123 487636, aizam@uthm.edu.my

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Abstract- When a digitally controlled grid-connected inverter's control loop has a time delay, phase shifts occur, which may lead to instability. The performance of a quadruple-sampled state-variable-derivative deadbeat current controller (QSSVDDCC) was compared with that of a typical PI controller in this research work. The comparison was conducted using MATLAB simulations. Both of these controllers were tested for their ability to tolerate changes in grid parameters. When compared with the PI controller, the QSSVDDCC exhibited superior resilience during both steady-state and transient conditions in mitigating a time delay of about 120 µs. Additionally, even at 80% grid-parameter variation, the QSSVDDCC demonstrated total harmonic distortion in current (THDi) of just 1.6%. It may be worthwhile to undertake an experiment to test the results of the simulations presented in this article further.

Keywords Time delay, Deadbeat control, Current control, Quadruple sampling and updating

1. Introduction

A distributed power generation system (DPGS) is an efficient method for making use of renewable sources of energy, such as wind and solar power[1][2], in order to mitigate issues of energy scarcity and environmental pollution [3]. However, the congestion on the transmission line poses a threat to power system operations. This issue has been researched and addressed using the gravitational search algorithm in [4], the elephant herd optimization in [5], the moth flame optimization in [6], the gravitational search algorithm in [7], and the modified grey wolf optimization algorithm in [8]. A grid-connected inverter is an essential component for injecting high-quality current into the utility grid because it serves as the interface for the power conversion process between the DPGS and the utility grid[9]. In grid-connected inverters, digital control has seen widespread use as a result of its simple hardware circuit, strong disturbance-rejection ability, and easy implementation of intricate control[10]. However, the digital solution does have a few shortcomings, the most problematic of which is the phase lag created in the control loop as a result of time delays. If more control loops are utilized, the delays will be amplified to a greater degree.

As a result of the presence of delays in the control loop, compensators are used to lessen or do away with the delays. The research community has come up with a number of different strategies for minimizing the effects of time delays, and these strategies may be categorized into model-based (MB) or model-free (MF) methodologies [11], [12]. Since the 1980s, among digital controllers, the deadbeat current controller (DBCC) has been garnering significant interest as a result of its many desirable characteristics, including zero steady-state error [13], [14], simple implementation on a digital control system, low current harmonics, rapid dynamic response [15], and robust time-delay compensation [3]. The deadbeat control has seen a wide range of applications, including power electronics control [16], [17], drive control of a permanent-magnet synchronous motor [18], [19], [20], control of power and active filters [21], [22], and resilient control protocol of the transmission line [23].

The proportional-integral (PI) controller, which is often implemented in a synchronous *dq* reference frame, is yet another kind of current controller that has seen widespread application [24][25]. During a balanced three-phase operation, the *dq0* transformation provides constant values, which enables the PI controller to do all of the necessary control actions. However, when operating in an unbalanced three-phase configuration, the values of *dq0* can fluctuate over time. This presents a challenge for the PI controller and may result in inaccurate readings [26]. In addition, the inability of this kind of controller to deal with time-varying signals and its low disturbance tolerance are also among its primary shortcomings. This approach becomes less appropriate for grid-connected inverters [27]. Due to the drawbacks of the PI controller, other types of controllers are used instead. The motivation underlining this research was connected to the recent research work conducted by [28], where an extensive analysis was undertaken on the five most prominent deadbeat controllers with time-delay compensation mechanisms. It was determined that the quadruple-sampled state-variable-derived deadbeat current controller (SVDDCC) provided good reference tracking, while also reducing time delays in the control loop. In addition, when quadruple sampling was added to the SVDDCC, as researched in [28], the time-delay mitigation was improved further, as suggested in [11]. The proposed controller was compared with a traditional PI controller. The main contribution of this paper is comparing the performance of the proposed QSSVDDCC with that of a PI-based controller. This comparison is novel because it has not been conducted in the past, based on the authors' intensive reading of the literature. The comparison focused on the THD, time-delay compensation, and robustness against grid parameter variation. The rest of this paper is organized as follows: The modeling of a three-phase grid-connected LCL inverter's system configuration is presented in Section 2, the proposed comparison between the QSSCDDCC's and the PI controller's designs is presented in Section 3, the simulation results and stability analysis is presented in Section 4, and the conclusion and recommendations is presented in Section 5.

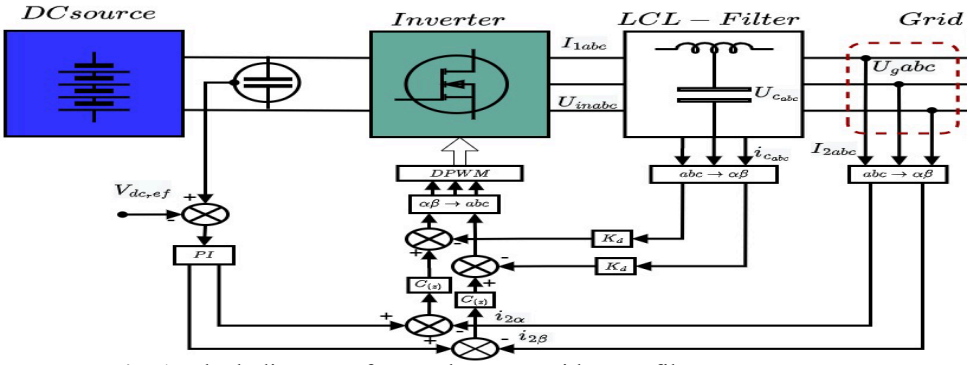

Fig. 1. Block diagram of control system with LCL filter

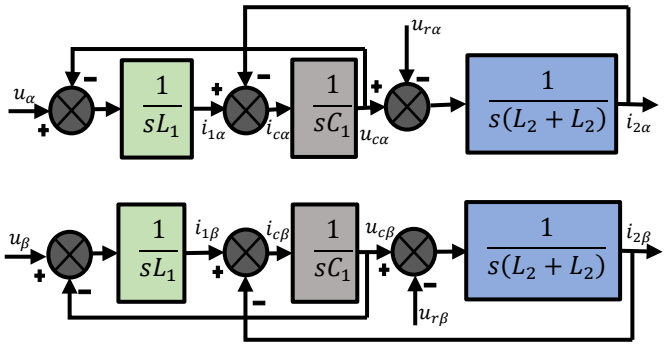

Fig. 2. Mathematical model of LCL filter in stationary reference frame

2. Modeling of Three-Phase Grid-Connected LCL Inverter

Figure 1 depicts the circuitry of an LCL inverter that is connected to the grid in three phases. In order to keep things as simple as possible, the series' parasitic elements are not taken into account in either the power components or the grid model. In Figure 1, $U_{in\ abc}$ is the output voltage of the inverter, $I_{1\text{abc}}$ is the inverter-side current, $I_{2\text{abc}}$ is the grid-side current, $U_{c\ abc}$ is the voltage of the capacitor, $I_{c\ abc}$ is the current of the capacitor, L_g is the impedance of the grid, and U_{gabc} represents the grid's voltage source. It is important to take note of the fact that if a three-phase system is symmetrical and balanced, then the electrical potentials of the capacitor terminal of the LCL and the lower terminal of the inverter are identical. Modeling the state equations of an LCL filter in the natural frame using Kirchhoff's voltage and current laws, the following results are obtained:

$$L_1 = \frac{d_{1k}}{dt} = U_{rk} - U_{ck},\quad C_1\frac{du_{ck}}{dt} = i_{1k} - i_{2k},\quad L_2 - L_g\frac{d_{1k}}{dt} = u_{ck} - u_k \Big\} \quad (1)$$

In today's world, a significant number of three-phase power converters are connected to power distribution systems that use three phases and three wires. Therefore, only two controllers are required because the third current is determined by Kirchhoff's current law. By using the Clarke transformation $[T_{\alpha\beta}]$ [27], the control loops of the system may be organized in the stationary reference frame, helping to make the control system less complicated.

$$T_{\alpha\beta} = \frac{2}{3}\begin{bmatrix}1 & -1/2 & -1/2\\ 0 & \sqrt{3}/2 & -\sqrt{3}/2\end{bmatrix} \quad (2)$$

When the Clarke transformation is applied, the state equations of the LCL filter in the stationary reference frame may be expressed as follows:

$$\left.\begin{aligned}\frac{d_{1a}}{dt} &= \frac{1}{L_1}u_{r\alpha} - \frac{1}{L_1}u_{c\alpha}\ ,\frac{1}{L_1}u_{r\beta} - \frac{1}{L_1}u_{c\beta}\\ \frac{du_{ca}}{dt} &= \frac{1}{C_1}i_{1\alpha} - \frac{1}{c_1}i_{2\alpha}\ ,\frac{du_{c\beta}}{dt} = \frac{1}{C_1}i_{1\beta} - \frac{1}{c_1}i_{2\beta}\\ \frac{d_{i2\alpha}}{dt} &= \frac{1}{L_2+L_g}(u_{c\alpha} - u_\alpha),\frac{d_{i2\beta}}{dt} = \frac{1}{L_2+L_g}\left(u_{c\beta} - u_\beta\right)\end{aligned}\right\} \quad (3)$$

Figure 2 depicts, in accordance with Equation 3, the mathematical model of the LCL filter when the stationary reference frame is considered.

3. Controller Comparison

The comparison was made based on a full-bridge three-phase inverter system using the parameters given in [10], as tabulated in Table 1. It is possible to exercise control over either the grid-side current or the inverter-side current of the LCL filter. There are disadvantages associated with both. Different active damping strategies have been presented, each of which is dependent on the regulated current. It can be observed that if the grid-side current is regulated, then the appropriate capacitor current active damping method is used. The idea of the suggested control strategy is illustrated by the entire block diagram that is shown in Figure 1, and from observation, the α and β phase angles have no cross-coupling terms, as shown in Figure 2. Therefore, the control structure can be discussed in terms of the α phase only without losing any form of generality. The control structure with only the α phase is depicted in Figure 3.

Table 1. Inverter parameters.

Rated power, p	80 kW
Switching frequency, f_s	10 kHz
Sampling frequency, f_{sw}	10 kHz
DC-link voltage, U_{dc}	680 V
Grid impedance, L_{gs}	0.012 mH
Inverter-side inductor, L_i	4.58 mH
Grid-side inductor, , L_g	0.92 mH
Grid-nominal voltage, U_g	230 V_{rms}
Filter capacitance, C_f	4.7 µF
Capacitor current damping factor, k_d	0.3157

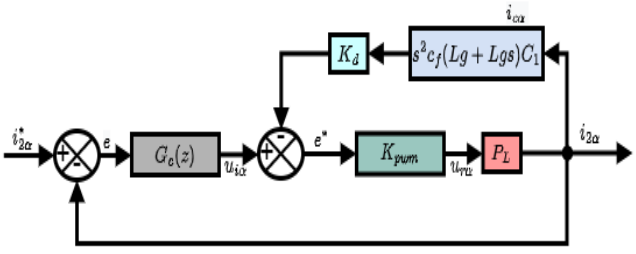

Fig. 3. Block diagram of grid-side control with active damping

As can be seen in Figure 3, $G_c(z)$ is the current controller; K_{pwm} is the gain of the full-bridge three-phase inverter [29], the approximation of which may be found in Equation 4; and k_d represents the damping factor of capacitor current. It is simple to construct the transfer function, P_L, that connects the grid-side current, $i_{2\alpha}$, and the inverter output voltage, $u_{i\alpha}$. This transfer function is expressed by Equation 5.

$$K_{pwm} = \frac{U_{dc}}{2} \tag{4}$$

$$T_{d(s)} = \frac{I_g}{U_c} = \frac{K_{pwm}}{s^3\left[L_i L_g{}' C_f\right] + s^2 K_{pwm} k_d C_f L_g{}' + s\left[L_i + L_g{}'\right]} e^{-1.5T_s s} \tag{5}$$

Using the parameters in Table 1, Equation 5 can be rewritten in a continuous and discrete form, as in Equation 6. Equation 6 serves as the delayed plant to be controlled. where $L_g{}' = L_g + L_{gs}$, in which L_{gs} is the grid-side inductor of the LCL filter and T_s is the sampling time.

$$\left.\begin{aligned} T_{d(s)} &= \frac{340}{2.006e^{-11}s^3 + 4.702e^{-7}s^2 + 0.005512s} e^{-1.5T_s s} \\ T_{d(z)} &= \frac{0.26158\,(z+11.81)(z+0.5335)(z+0.02728)}{(z-1)(z^2 - 0.2404z + 0.09597)} z^{-2} \end{aligned}\right\} \tag{6}$$

3.1. *Quadruple-Sampled State-Variable-Derivative Deadbeat Current Controller (QSSVDDCC)*

The pulse transfer function from the output to the input, as depicted in Figure 4, is expressed by Equation 10, where *A*, *B* and *C* are state matrices, while K^T and K_W are constants that perform the control actions.

$$\frac{Y_{(z)}}{E_{(Z)}} = C^T\left[[zI - A] + BK^T\right]^{-1} BK_W \tag{10}$$

The state-space control's canonical version of the pulse transfer function, as defined by Equation 6, is as follows:

$$A = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0.3839 & -0.6728 & 1.241 \end{bmatrix} \quad B = \begin{bmatrix} 0 \\ 0 \\ 2 \end{bmatrix}$$

$$C = [0.2616 \quad 1.648 \quad 1.78], D = [0.2616]$$

$$K^T = [k1 \quad k2 \quad k3]$$

$$X_c = \left[[z * I - A] + B * K^T\right] \tag{11}$$

Let's designate K^T as the constant that must be used in order to position the poles at the origin, and X_c as the characteristic polynomial according to Equation 11. In this study, in order to determine the K^T matrix, a comparison was carried out between Equation 11 and the necessary polynomial that was located at the origin, without losing any form of generality. The K^T matrix was found to be:

$$K^T = [0.19195 \quad -0.33641 \quad 0.62]$$

To obtain the second constant, which was required to place the poles at the origin, Equation 10 was used for unity gain, and it was obtained as:

$$K_w = 0.18951$$

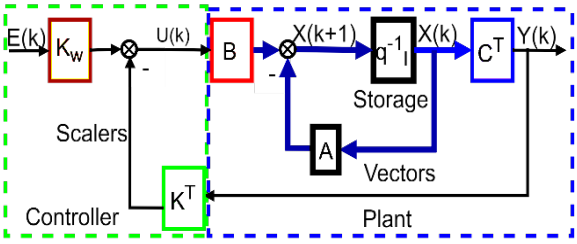

Fig. 4. Block diagram of QSSVDDCC with inverter

Having obtained all the parameters required, the overall closed-loop state matrix was obtained as:

$$A = \begin{bmatrix} 0 & 0.5 & 0 \\ 0 & 0 & 0.5 \\ 0 & 0 & 0 \end{bmatrix}, B = \begin{bmatrix} 0 \\ 0 \\ 0.3789 \end{bmatrix}$$

From this new state matrix, the deadbeat controller and the overall transfer function were obtained as Equations 12 and 13, respectively.

$$DB_{s(z)} = \frac{2.578z^5 - 2.004z^4 - 0.5606z^3 + 0.09092z^2 - 0.0974\,z - 0.004857}{z^6 + 12.37z^5 + 6.636z^4 + 0.1719z^3} \tag{12}$$

$$\frac{Y_{(z)}}{E_{(z)}} = \frac{0.6744(z+0.4152)(z+0.04728)}{z^5} \tag{13}$$

3.2. *PI Controller*

Figure 5 shows the block diagram of the PI controller and Equation 7 expresses the plant ($P_{(z)}$), controller $C_{(z)}$ and the characteristic equation ($n_{(z)}$), while $D_{(z)}$ represents the external disturbance.

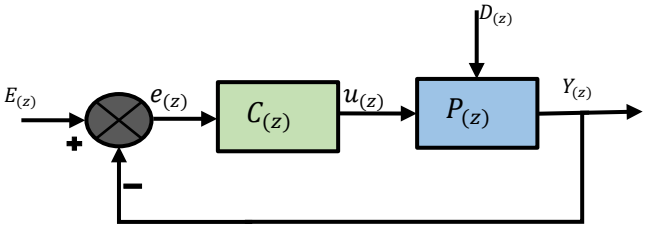

Fig. 5. Block diagram of PI controller

$$\left.\begin{aligned} G_{(z)} &= \frac{N_{P(z)}}{D_{P(z)}} \\ C_{(z)} &= \frac{N_{C(z)}}{D_{C(z)}} \\ n_{(z)} &= D_{P(z)} \times D_{C(z)} + N_{P(z)} \times N_{C(z)} \end{aligned}\right\} \tag{7}$$

For the digital PI controller, the following equation holds:

$$C_{(z)} = K_p + K_i T \times \frac{z}{z-1} = (K_p + K_i T)\left(z - \frac{K_p}{K_i T + K_p}\right) \quad (8)$$

Equation 8 can be further simplified, as in Equation 9.

$$C_{(z)} = k_1 \frac{(z - k_2)}{z - 1} \quad (9)$$

where $K_p = K_1 K_2$ and $K_i = \frac{K_1 - K_1 K_2}{T}$.

By putting the controller expression into the characteristic equation and comparing with the desired poles at the origin, the following values were realized:

$Kp = 0.3; Ki = 20$

4. Simulation Results

Figure 6 shows the simulation diagram, while Figure 7 shows the power injected into the grid by the PI controller and the QSSVDCC. About 20 kW of power was injected by both controllers. More overshoots were noticed on the power injected by the PI controller as compared with those by the QSSVDCC. Figure 8 shows the superimposed output currents of the two controllers, where I_{api} represents the output current from the PI controller and I_{aqs} represents the output current from the QSSVDCC. From a closer view of the signals in Figure 8(a), one can observe the mitigation of about 120 µs of time delay by the QSSVDCC as compared with that of the PI controller. Figure 8(b) shows the difference and the tolerance between the two signals from the two controllers, where it can be observed that at the point of transient to the Load B mode from the Load A mode, the PI controller exhibited an overshoot of about 25%, while the QSSVDCC exhibited an overshoot of less than 5%. At the point away from the Load B mode, the PI controller exhibited a low distortion in current, while the QSSVDCC did not show any distortion. Figure 8(c) shows a closer view of the signals at the point of hooking and falling of the grid, where the QSSVDCC signal led the PI signal by about 120 µs.

Figure 9 shows the superimposed output voltages of the different controllers, where V_{api} represents the output voltage from the PI controller and V_{aqs} represents the output voltage from the QSSVDCC. As seen from a closer view in Figure 8(a), the voltage from the QSSVDCC led the voltage from the PI controller by about 120 µs, and a low distortion in voltage can be seen during the grid-connected mode as compared with the distortion in the current from Figure 8(a). Figure 9(b) shows the difference and tolerance between the two controllers' voltages. From a closer inspection, there was a low voltage distortion from the QSSVDCC at the point of connection to the grid, while for the PI controller, it was not noticed, as seen in Figure 9(c).

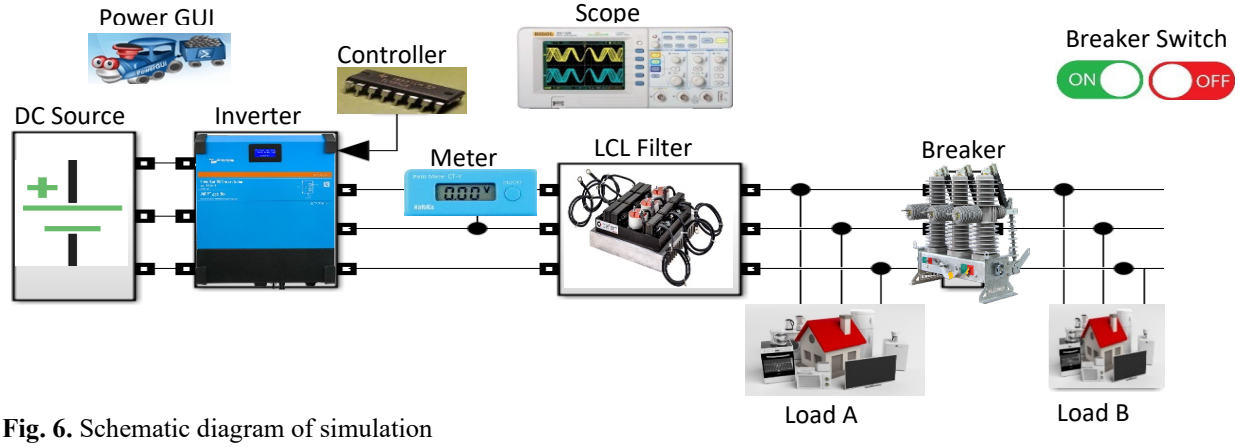

Fig. 6. Schematic diagram of simulation

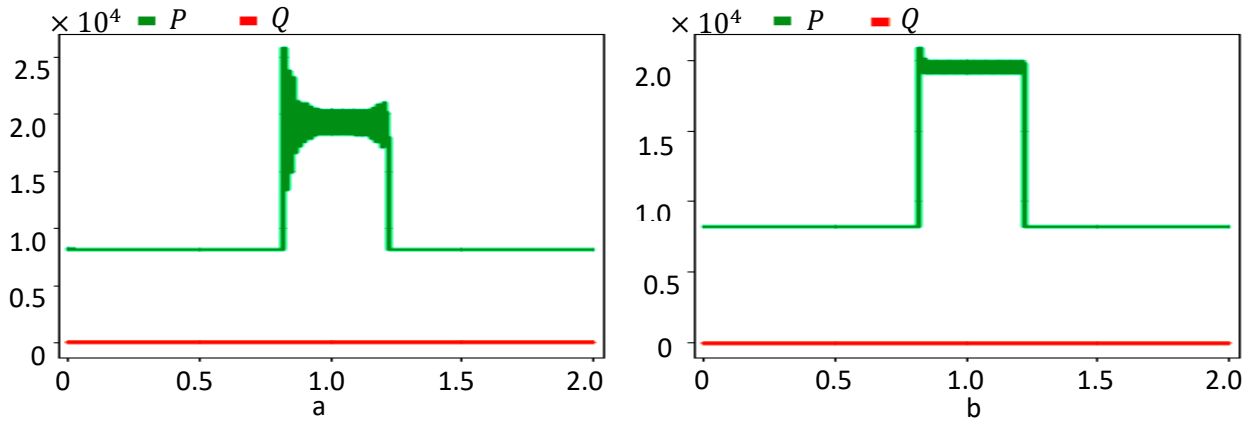

Fig. 7. Output power: (a) PI controller and (b) QSSVDCC

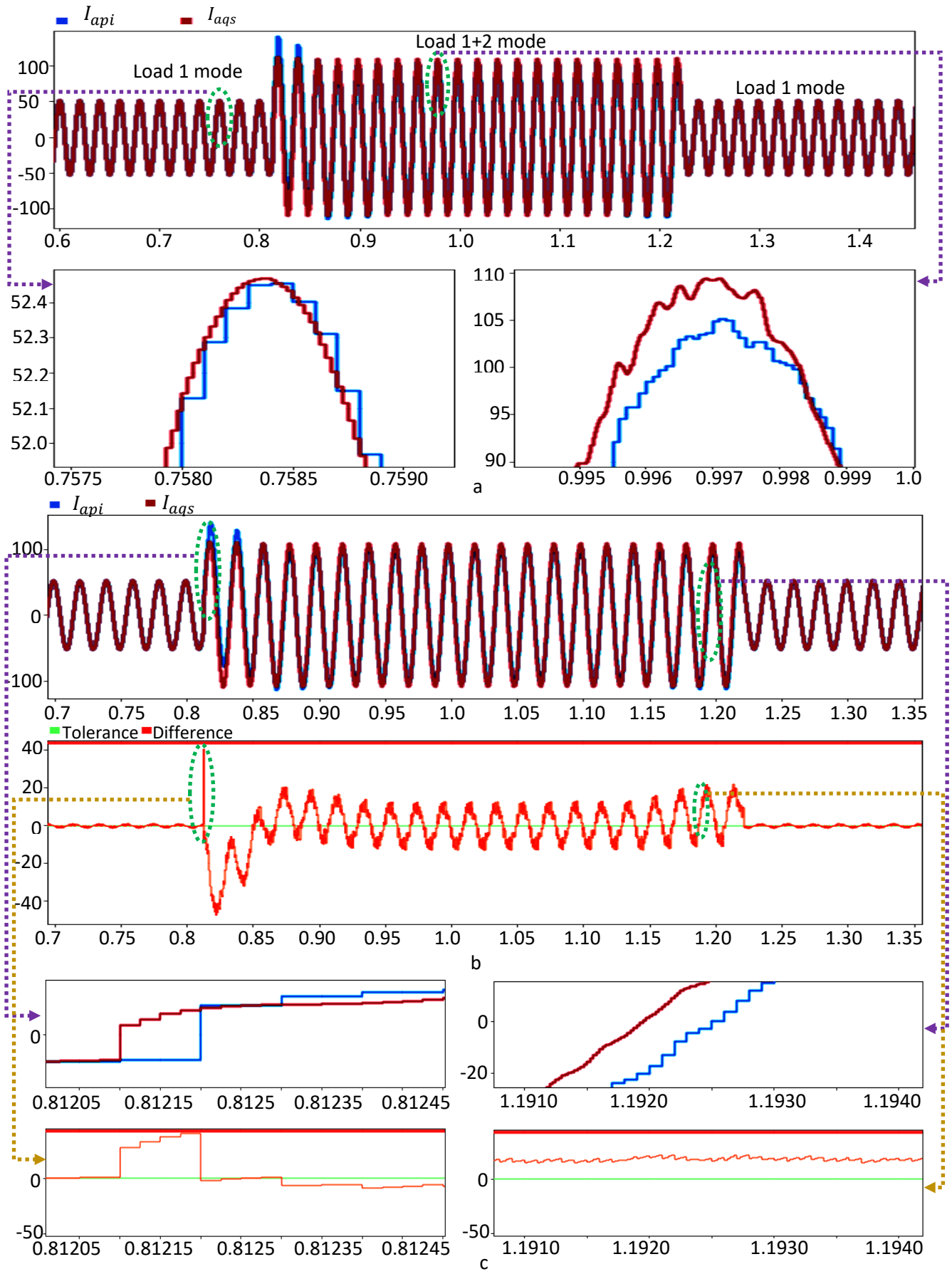

Fig. 8. Super-imposed output currents of PI controller and QSSVDDCC

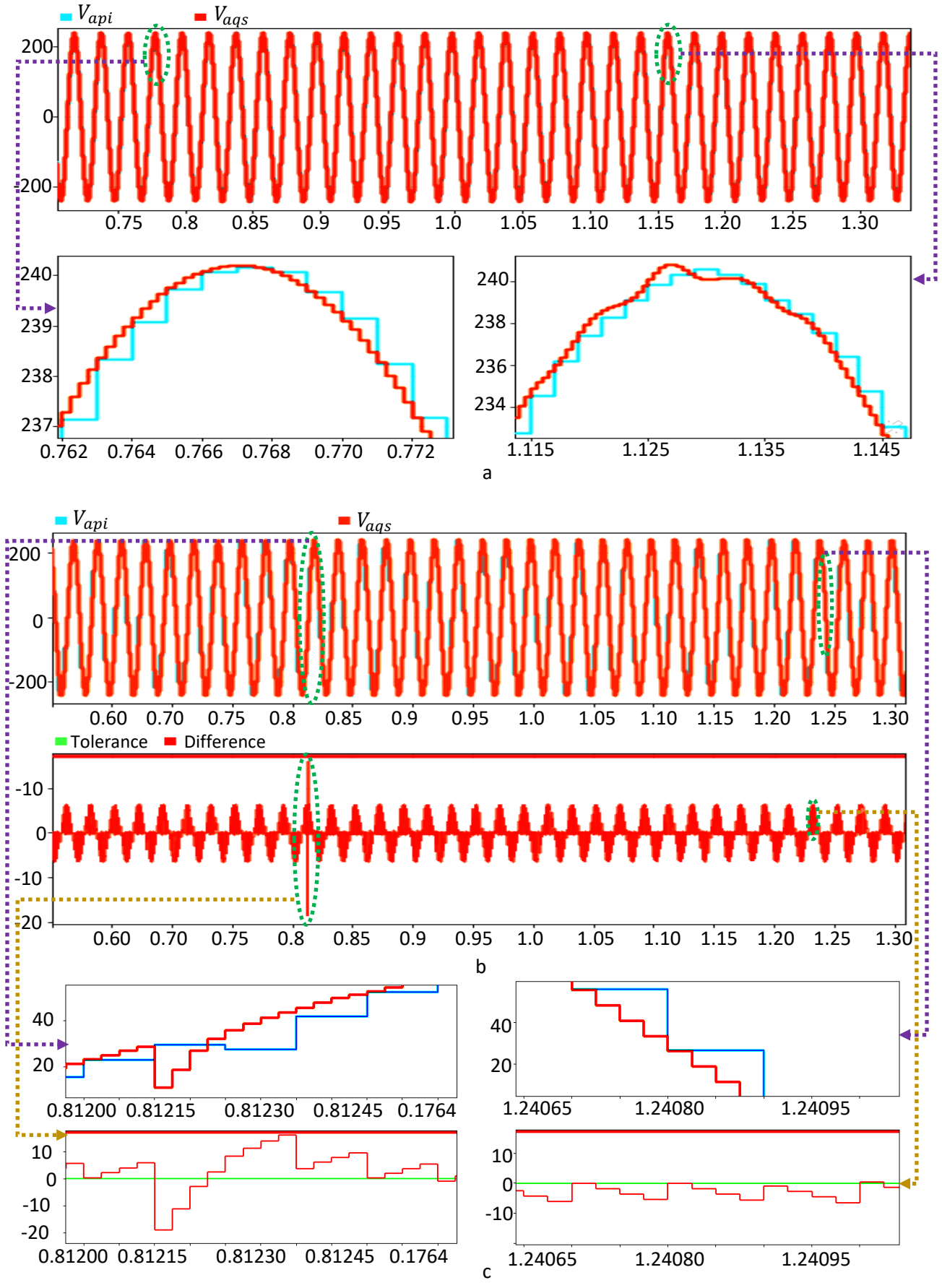

Fig. 9. Super-imposed output currents of PI controller and QSSVDDCC

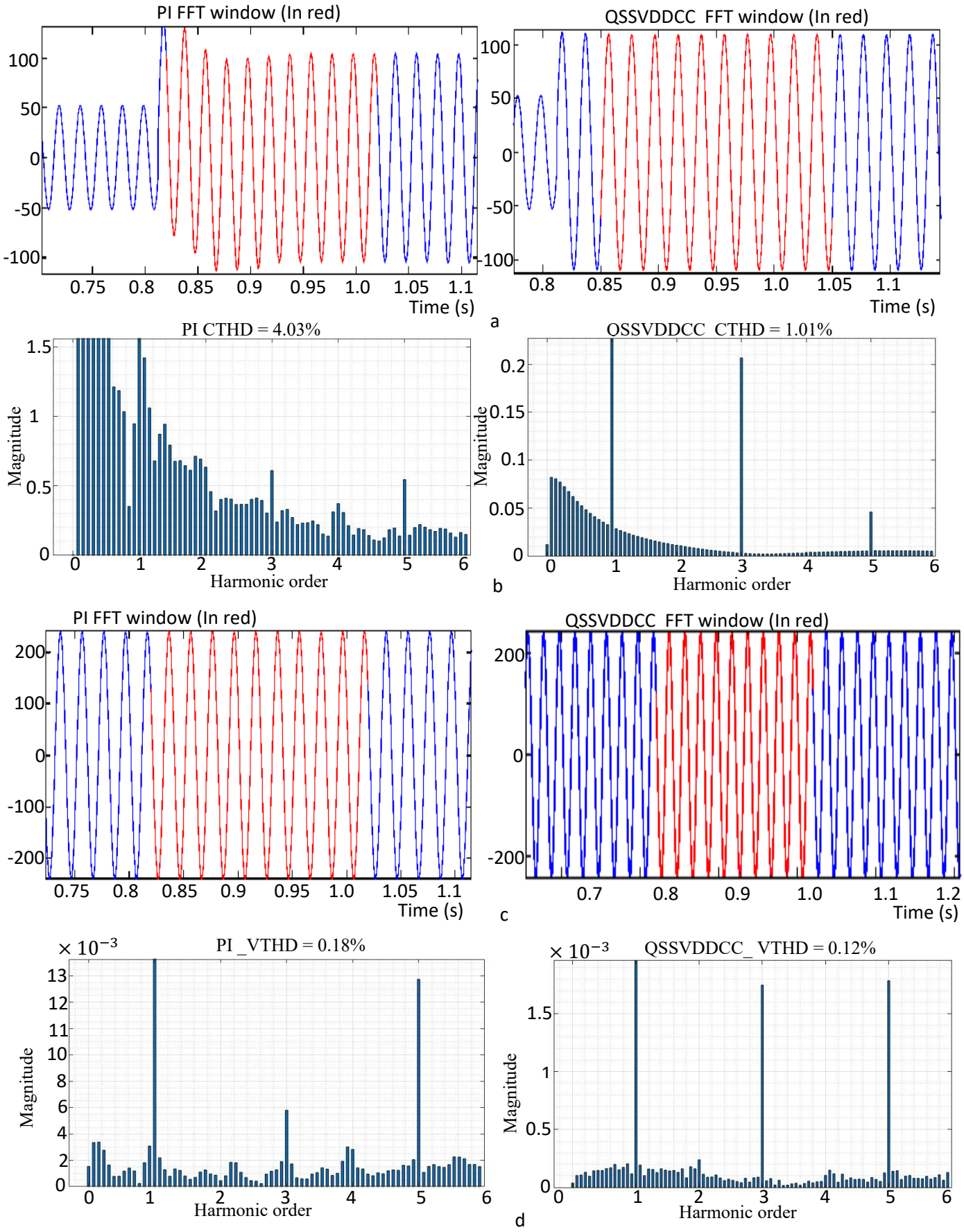

Fig. 10. Current and voltage THD of PI controller and QSSVDDCC

Table 2. THD parameters.

Controllers	THDi (%)	THDv (%)
At steady state		
PI	4.03	0.18
QSSVDDCC	1.01	0.12
At 40% grid-impedance variation		
PI	6.02	0.58
QSSVDDCC	1.34	0.41
At 80% grid-impedance variation		
PI	9.2	1.05
QSSVDDCC	1.6	0.92

Figure 10 depicts the current and voltage THD of the two different controllers under investigation, Figure 10(a) shows the current waveform, while Figure 10(b) shows the THDi spectrum, where the PI controller exhibited THDi of 4.03%, while the QSSVDDCC exhibited THDi of 1.01%. Figure 10(c) and (d) show the voltage and THDv of the two controllers, respectively. The PI controller showed THDv of 0.18%, while the QSSVDDCC showed THDv of 0.12%. Both the THDs at steady state were within the acceptable limit of the IEEE standard.

Table 2 summarized the THDs of the two controllers both at steady state as well as during grid-impedance perturbations of 40% and 80%. It is evident from the values in the table that at steady state, both controllers' THDs were within the acceptable limit. However, at 40% and 80% variations, the PI controller exhibited THDi above the threshold set by the IEEE. In contrast, for the QSSVDDCC, despite the variations, both current and voltage THDs were within the acceptable limit, which demonstrates the effectiveness of the proposed method.

5. Conclusion

In this research work, an intuitive comparison of the performances of the PI controller and the QSSVDDCC was conducted. The QSSVDDCC is known to have a better time-delay mitigation ability and robustness against grid-parameter variation as compared with other deadbeat current control methods. Both controllers were tested on a full-bridge inverter with an LCL output filter, and the results were obtained based on MATLAB simulations. According to the findings from the figures, as well as the THD table, the QSSVDDCC showed a reduced delay of approximately 120 microseconds in comparison with that of the PI controller during both the transient operation and the steady-state operation. In addition, the QSSVDDCC demonstrated a low level of distortion for both current and voltage when operating in either grid mode or islanded mode during both steady-state and transient conditions. Moreover, the QSSVDDCC showed minimum THDi of 1.6% at 80% variation in grid parameters. It may be inferred that the QSSVDDCC design method is a competent solution for mitigating time delays in the control loop of a grid-connected inverter.

In conclusion, the QSSVDDCC design demonstrated not only excellent performance but also robustness against alterations in the parameters. Future works may include investigating additional deadbeat control design strategies, as well as conducting an experimental test to better validate the current study.

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