A Novel Transformerless Inverter Topology without Zero-Crossing Distortion

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Abstract- The elimination of the transformer in solar photovoltaic inverters has reduced the size, the weight and the losses in the system. On the other hand, the galvanic connection between the DC source and the grid generates leakage current through the earth parasitic capacitance. The leakage current depends on both the inverter topology and the control strategy. Among the existing inverters is the Highly Efficient and Reliable Inverter Concept (HERIC) topology that has low leakage current level and high efficiency. However, this topology suffers from low frequency harmonics and current zero crossings distortions. To eliminate these harmonics and distortions, a new transformerless inverter is proposed. The design is a conventional full bridge inverter with an extra AC bypass. The bypass branch disconnects the inverter from the grid during the freewheeling period. Simulation results indicate that the zero crossings distortions are totally eliminated and that the low frequency harmonics are significantly reduced as a result of the appropriate applied control. Moreover, losses analysis of the proposed design yields an efficiency of up to 94.14% and shows that the topology meets relevant standards.

Keywords- PV, inverter, transformerless, common mode voltage, leakage current, ripples, harmonics, zero crossings distortions.

1. Introduction

Photovoltaic inverters can be divided into three main system configurations: central inverters, string inverters and module integrated inverters [1]. The central and string inverters are based on the series and parallel connections of many photovoltaic panels by means of long DC cables and they exhibit problems such as:

- Mismatching losses by using one maximum power point (MPP) control for a large group of PV modules.
- Extra losses and risk of electrical arc in the long DC wiring.
- Limited design flexibility.

Subsequently, the module integrated inverters are being developed to overcome the above problems. Each PV system has its dedicated small-sized inverter mounted on the back of panel [2,3,4,5]. Therefore, mismatching losses are significantly reduced since each module has its own MPP tracking circuit. DC wiring is minimized and the safety of the entire PV system is improved. In this case, the transformer which is heavy, bulky and inappropriate for individual solar

panel installation would not be a requirement. Therefore, new transformerless topologies have been developed and commercially available. However, the transformerless inverter creates a common-mode resonant circuit including the filter, the inverter, the impedance of the grid and the DC source ground parasitic capacitance. In this case, a common-mode current is generated and superimposed to the grid, hence increasing its harmonics content [6,7] and causing an electromagnetic interference (EMI) between the PV system and the grid [8,9,10]. In addition, even though, the transformer ensures galvanic isolation between the grid and the PV system and provides protection and suppresses the leakage current between the PV and the earth, its omission significantly increases the efficiency of the entire system [11-12].

Accordingly, many standards have been deployed to set a maximum allowed leakage current [10,13]. For instance,

the German DIN VDE 0126-1-1 mandates that a leakage current of 30mA necessitates the disconnection of the inverter from the grid within 0.3 second. Other standards, such as IEEE 929-2000, IEC 61727, IEEE 1547, and EN 61000-3-2 have set the maximum DC current injected to the grid to be between 0.5 % and 1%.

From the power quality point of view, standards such as the IEC61000-3-2 and the IEEE 519-1992 [13,14] have set the THD level to less than 5%.

In this paper, a new transformerless inverter topology with a high efficiency, a low total harmonic distortion (THD), low leakage current, and no zero crossings distortions is presented.

The novel topology is based on the conventional full bridge with two extra switches at the AC side. This extra branch disconnects the inverter from the load when the zero voltage of the PWM is applied to the load. Hence, it helps keeping the power with the load which increases the efficiency of the whole system. Besides, the DC current injected to the grid is significantly reduced so does the leakage current through the parasitic capacitance.

Section II reviews the well-known topologies, with a special focus on the HERIC topology. In section III, the zero crossings distortions (ZCD) phenomenon is introduced. Section IV presents a detailed study and simulation of the HERIC topology, while section V describes the efficiency analysis and the simulation of the proposed topology. Section VI recapitulates the results of the analysis and simulation results. Conclusions and future work are summarized in Section 7.

2. Review Of Transformerless Inverter Topologies

Ideal transformerless inverter generates constant common mode voltage. However, if the voltage varies with time, then a leakage current is produced. For the sake of minimizing this leakage current, different topologies were studied in details [1, 3, 4, 8, 11, 15,16]. Among these are the full bridge with bipolar PWM, the half bridge, HERIC, H5, H6 and NPC all of which experience certain drawbacks which are discussed next.

2.1. Full Bridge Inverter

The full-bridge inverter with bipolar PWM [6, 15,16] causes high switching losses and large current ripples and does not eliminate the DC current injected into the grid that has the tendency of saturating the transformer cores. Even though, this topology is being used in some commercial transformerless inverters, it still presents quite low efficiency according to the European standards due to the losses caused by the double switching frequency [8].

2.2. Half Bridge Inverter

The half bridge inverter, on the other hand, requires a high input voltage and a boost converter in the DC side that would increase the inverter size and cost and reduce its efficiency down to 92% [6,8]. For this reason the half bridge is not recommended.

2.3. HERIC Inverter

Meanwhile, as detailed in [3, 15], the HERIC topology, shown in Fig. 1, combines the advantages of the unipolar and bipolar modulations. It has a three level output voltage, a high efficiency and a low leakage current. However, the HERIC topology presents low frequency harmonics and does not allow for reactive power flow. This is due to the control strategy.

2.4. H5 Inverter

This topology is based on the full bridge with an extra switch on the DC side. In this topology, the upper switches operate at grid frequency while the lower switches operate at high frequency [16,17]. The extra switch operates at high frequency and guarantees the disconnection of the DC source from the grid. This topology has two main disadvantages. The first one is the high conduction losses due to the fact that three switches operate simultaneously. The second one is that the reactive power flow is not possible due to the control strategy [16].

2.5. NPC Inverter

The NPC inverter topology is being considered as an attractive solution in case of transformerless systems. This inverter has the advantages of no internal reactive power flow, a three level inverter output voltage and a low leakage current [6,16]. However, it requires an input voltage as high as twice the input voltage required by other topologies and a boost stage which increases inverter losses and size.

2.6. Flying Inductor Inverter

The Flying inductor inverter is also known as the Karschny inverter. It consists of a buck-boost circuit and an inverter and requires additional semiconductor devices in the current path as well as high inductors to store the entire inductive energy [16]. These additional components reduce the overall efficiency and increase the cost and size of the inverter.

3. Review Of Zero-Current Crossing Distortion

The zero-current distortions are known to cause damage to certain equipment such as computers and televisions [14]. It looks like a notch taken out of the sine wave near the zero-crossings. In this case, the inverter current waveform can be described as a superposition of a pure sine wave to which a distorting wave form d(x) is added. This waveform is analytically represented as follow:

$$d(x)=\begin{cases}0, x\in\left[0,\pi-\theta_{ZCD}\right]\cup\left[\pi,2\pi-\theta_{ZCD}\right]\\ -\sin(x), x\in\left[\pi-\theta_{ZCD},\pi\right]\cup\left[2\pi-\theta_{ZCD},2\pi\right]\end{cases} \quad (1)$$

In this equation, θ_{ZCD} is the zero-crossings distortions notch angle.

Fourier analysis of this wave form is used to find the coefficients (a_n and b_n) and the harmonics that cause the electromagnetic emission and interference by the inverter, and to design the proper filter [14].

$$a_n=\begin{cases}\frac{1}{\pi}\left(\frac{1}{n-1}-\frac{1}{n+1}-\frac{\cos(n-1)\theta_{ZCD}}{n-1}+\frac{\cos(n+1)\theta_{ZCD}}{n+1}\right), \text{for n} = 3,5,7,\ldots\\ \frac{1}{2\pi}\cos\left(2\theta_{ZCD}-1\right), \text{for n} = 1\end{cases} \quad (2)$$

and

$$b_n=\begin{cases}\frac{1}{\pi}\left(\frac{sin(n-1)\theta_{ZCD}}{n-1}-\frac{cos(n+1)\theta_{ZCD}}{n+1}\right), \text{for n} = 3,5,7,\ldots\\ \frac{1}{2\pi}\left(2\theta_{ZCD}-sin2\theta_{ZCD}\right), \text{for n} = 1\end{cases} \quad (3)$$

The magnitude M*n* of the nth order harmonic defined in (4) is a function of the harmonic's number n and the zero-crossing angle $\theta_{ZCD.}$

$$M_n=\sqrt{a_n^2+b_n^2} \quad (4)$$

The zero-crossings distortions create inductor-voltage spikes. These spikes are produced because of the sudden change in the current during the zero-crossing period. For sensitive power semiconductor devices, excessive current can flow if the voltage spikes exceed the breakdown voltage of the semiconductor devices.

This zero crossings distortions are due to many phenomena, one of which is the coincidence of the switching frequency with the filter resonance frequency [18]. However, the control strategy of the inverter is the main source of such distortions.

So far, different topologies were discussed in light of the issues associated with the reviewed topologies such as leakage current and zero-crossings distortions.

The HERIC topology that has many features will be used as a reference hereafter. Therefore; the following section presents a detailed study and simulation of the HERIC inverter.

4. HERIC Transformerless Inverter Topology

4.1. HERIC topology Common Mode Current

For the HERIC topology, shown in Fig.1, the common-mode voltage (v_{cm}) and current (i_{cm}) through the capacitance CGPV between the photovoltaic array and earth are:

$$v_{cm}=\frac{v_{AO}+v_{BO}}{2} \quad (5)$$

And

$$i_{cm}=C_{GPV}\frac{dv_{cm}}{dt} \quad (6)$$

Voltages v_{AO} and v_{BO} are controlled by the four switches (S_1throughS_4).

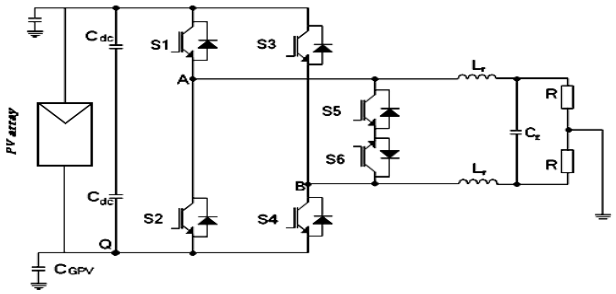

Fig.1. HERIC topology.

When the upper switch S_1 or S_3 is ON, the corresponding voltage is v_{IN}. However, when the lower switch S_2 or S_4 is ON, the corresponding voltage is zero. During the positive half wave, S_6 is turned ON and is used in the freewheeling period of S_1 and S_4. When both S_1 and S_4 are ON, $v_{AO}=v_{IN}$ and $v_{BO}=0$. Therefore, the applied common mode voltage is:

$$v_{cm}=\frac{v_{IN}}{2} \quad (7)$$

Table 1. Exhibits the switching principle of the HERIC inverter topology and shows that vcm is always constant.

Vector	*N*	*P*	$i_{grid}<0$	$i_{grid}>0$
S1	OFF	OFF	OFF	OFF
S2	ON	OFF	OFF	OFF
S3	ON	OFF	OFF	OFF
S4	OFF	ON	OFF	OFF
S5	OFF	OFF	ON	OFF
S6	OFF	OFF	OFF	ON
v_{AO}	0	VIN	NA*	NA*
v_{BO}	v_{IN}	0	NA*	NA*
v_{cm}	½v_{IN}	½v_{IN}	≈½v_{IN}	≈½v_{IN}

*Not Applicable (NA)

Therefore, according to equation 2, the common mode current i_{cm} is zero.

The performance of the HERIC inverter in terms of icm and icm was simulated using non ideal power electronic devices and the results are shown in Fig. 2.

It is clear that the common mode voltage is small and the leakage current is low. However, if the switching actions take place simultaneously, then the common mode voltage would be totally eliminated [17].

During the freewheeling period, S1 and S4 are turned off, vAO decreases to zero and vBO increases until the diode of S5 switches ON. If during the switching process, the magnitude of the increase in vBO is equal to that of the vAO decrease, then Vcm satisfies equation (7).

During toff, the inductor current flows through S6 and the diode of S5. The voltage applied to the inductor is (-vgrid) [8], vAO=0, vBO=vIN and the common mode voltage is:

$$v_{cm}=\frac{v_{IN}}{2} \tag{8}$$

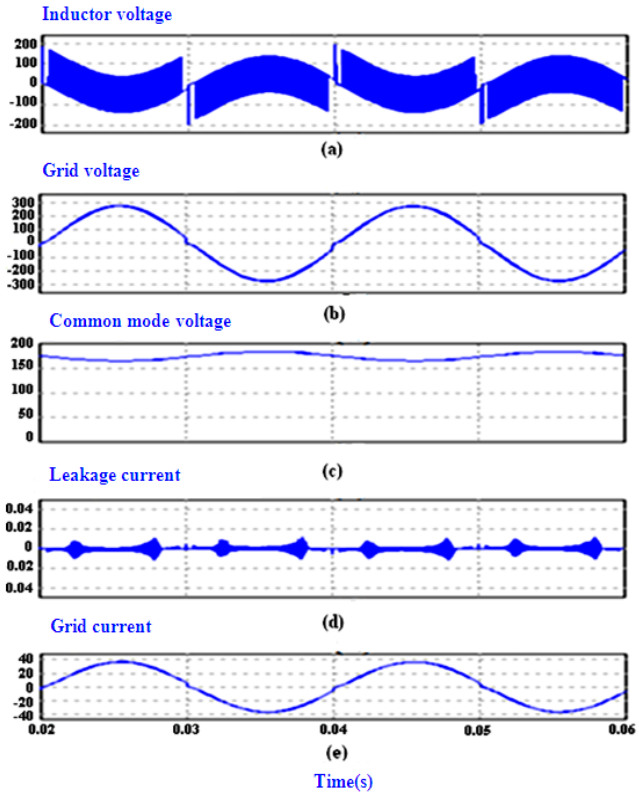

Fig.2. HERIC topology simulation results.

4.2. HERIC topology Zero Crossings Distortions

For the HERIC inverter topology, the simulation results depicted in Fig. 2 (b and e) show a short break of 0.8 ms at the current zero-crossings. In this topology, the main switches utilize the PWM control strategy. The AC bypass branch operates at the line-frequency switching order. Despite the fact that this reduces losses, it also interrupts the current flow near the zero crossings and the current may not be well controlled there, which results in a distorted waveform and inductor voltage spikes as shown in Fig.2 (a).

However, these issues can be solved with improved control strategies and topologies that present smooth four-quadrant operation near the zero crossings [14].

5. Proposed Transformerless Inverter Topology

5.1. Topology and Principles of Operation

The proposed topology is shown in Fig. 3 and consists of six IGBTs, six freewheeling diodes and one diode-bridge on the AC side.

The switching principles are similar to those of the HERIC topology presented in Table 1, except for the high switching frequency of S5 and S6. During the positive grid period, S1 and S4 are switched ON and OFF at a high switching frequency, while S6 is OFF and ON, respectively. In this case, when S1 and S4 are turned OFF, the freewheeling current finds its path through D3, S6 and D2 as indicated by the dotted line in Fig. 4 and Fig.5. For the negative half cycle, the freewheeling path is through D1, S5 and D4.

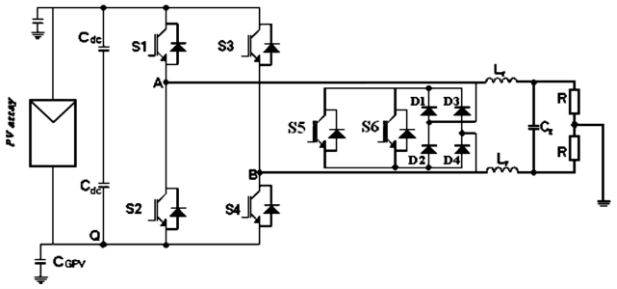

Fig.3. Proposed transformerless inverter topology.

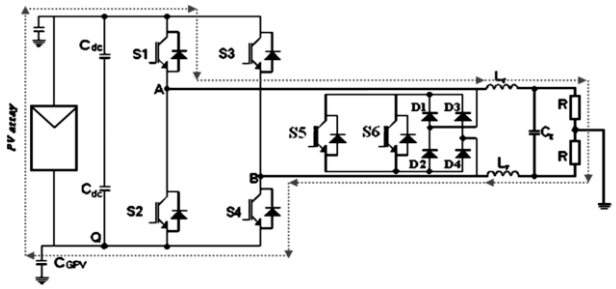

Fig.4. Proposed topology showing the current path during the positive half cycle (dotted line).

5.2. Leakage Current and Zero Crossing Distortions

For the proposed inverter topology, the simulation results are included in Fig. 6 and show that the leakage current does not exceed 21.10 mA, which is within the 30 mA limit set by the DIN VDE 0126-1-1standard.In fact, the common mode voltage varies from 165 V to 184 V. This variation is low and leads, therefore, to a low leakage current level. In addition, the zero crossings distortions are eliminated.

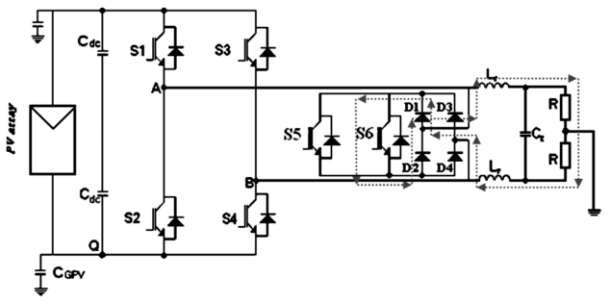

Fig.5. Proposed topology showing the current path during the freewheeling period of S1-S4 (dotted line).

In the AC side, the bypass branch switches at the same frequency of S1-S4.This means no sudden switching exists at the end of each half cycle and the bypass branch does not interrupt the flow of current. Therefore, the inductor voltage

spikes would not appear as shown in Fig.6 (a). Such a control strategy also eliminates the zero-crossings distortions as shown in Fig. 6 (b and e), but at the expense of a small increase in the current ripples which can be easily removed using a simple EMI filter.

5.3. Efficiency

The efficiency of the proposed topology was estimated based on the power switches losses: switching, and ON-state losses.

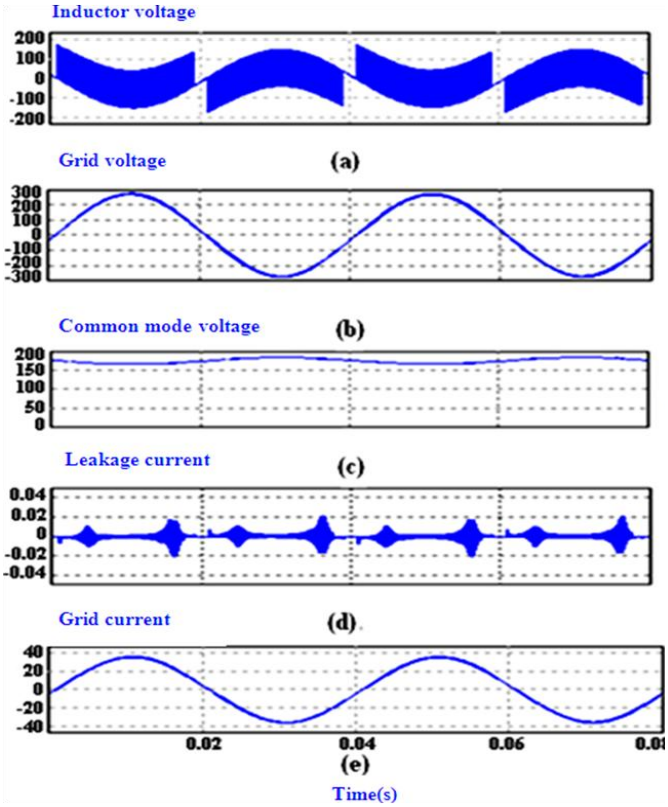

Fig.6. Proposed topology simulation results.

IGBT Switching Losses

The total switching power losses (P_{tot-sw}) can be defined as the ratio of the total switching energy losses (E_{tot}) over the switching period. E_{tot} is usually specified in the device datasheet and includes both switching and diode reverse recovery energy losses. Then, P_{tot-sw} can be defined as:

$$P_{tot-sw} = f_s E_{tot} \tag{9}$$

By convention, the switching energy available in the datasheets is for a specified test voltage and current (V_{test} and I_{test}). To account for actual operating voltage and current, a correction coefficient (Y_0) is needed and the switching losses are expressed as [19, 20]:

$$P_{tot} = (P_{tot})_{Datasheet} Y_0 \tag{10}$$

With:

$$Y_0 = K_g \frac{V_{bus}}{V_{test}} \frac{I_0}{I_{test}} = \frac{1}{\pi} \tag{11}$$

Where K_g, V_{bus} and I_0 are the correction factor, bus voltage and peak load current, respectively.

Combining the above three equations yields the following equation for the IGBT switching power losses:

$$P_{tot-sw} = \frac{f_s E_{tot(Datasheet)}}{\pi} \tag{12}$$

IGBT Conduction Losses

The ON-state power losses for one switch and for the freewheeling diodes are [21]:

$$P_S = \frac{N}{T_g}\left(I_L V_{ce}(dT - (t_r + t_f + t_{d-on} + t_{d-off}))\right) \tag{13}$$

And

$$P_{fd} = \frac{N}{T_g}\left(I_L V_F((1-d)T - (t_r + t_f + t_{d-on} + t_{d-off}))\right) \tag{14}$$

where:

I_L: *load current, RMS value.*
V_{ce}: *IGBT emitter to collector voltage.*
d: *duty cycle.*
f_s: *switching frequency.*
T_s: *switching period.*
T_g: *grid period.*
t_r: *rise time.*
t_f: *fall time.*
$t_{d\text{-}off}$: *turn-off delay time.*
$t_{d\text{-}on}$: *turn-on delay time.*
V_F: *diode forward voltage drop.*
N: *Switching times per grid cycle.*

Diode Power Losses

Since the power dissipated by each diode during one switching period is not provided in the datasheet, it must be estimated. In fact, the power dissipated in one diode is the sum of the power dissipated during the on-state phase, the off-state phase and the commutation phase [22,23].The diode power losses during the ON-state and the OFF state and the diode reverse recovery losses are respectively:

$$P_{on} = I_F V_F d \tag{15}$$

$$P_{off} = I_R V_R (1-d) \tag{16}$$

$$P_{rec} = \frac{1}{2} V_R Q_{rr} f \tag{17}$$

Where Q_{rr} is provided in the device datasheet and defined as [23]:

$$Q_{rr} = K_{Qr}\sqrt{I_F} \tag{18}$$

where:

K_{Qr}: *a function of di/dt.*
I_F: *diode forward current.*

V_F: *diode forward voltage.*
I_R: *diode reverse current.*
V_R: *diode reverse voltage.*
Q_{rr}: *reverse recovery charge.*
f_s: *switching frequency.*

Combining (12) through (19) yields the total power losses of the semiconductor devices-IGBT and AC bridge diodes, as shown below:

$$P_{total} = 3P_{tot-sw} + 3P_S + 3P_{fd} + 2(I_L V_F d + I_R V_R (1-d) + \frac{1}{2} V_R Q_{rr} f_s) \quad (19)$$

6. Results

The above equations are used to estimate the losses of the proposed topology as well as those of the HERIC topology. In the losses estimation, six non-ideal IGBTs (IRG4PH50KD) and four non ideal diodes (HFA30PB120) from the HEXFRED family are used. The parameters of selected switching devices are listed in Table 2 while the estimated losses are given in Table 3.

Table 2. Power Loss Estimation Parameters

Parameter	Value	Unit
$I_{L,rms}$	25.22	A
V_{ce}	2.77	V
d	50.00	%
T_g	20.00	ms
t_f	390	ns
$t_{d\text{-}off}$	67	ns
$I_{PV,avg}$	14.38	A
V_{DC}	350	V
$t_{d\text{-}on}$	310	ns
V_F	2.30	V
N	160	
I_R	1.50	mA
V_R	800	V
Q_{rr}	1838	nC
f_s	8	kHz
t_r	0.72	ns

From Table 3, it is clear that the conduction losses for the proposed topology are lower than those of the HERIC topology. This is due to the fact that, for the HERIC topology, one switch (S_5 or S_6) and one freewheeling diode remain ON during the entire grid half cycle. However, in the proposed topology, these switches are subject to grid current for much shorter time. On the other hand, even though there are additional diodes losses, the overall losses in the proposed topology were almost equal to and even a bit lower than those of the HERIC and therefore, a slight improvement in the overall efficiency is obtained. Further improvement is possible to achieve if better diodes with lower power losses are used.

The proposed inverter topology has several features, namely the elimination of the zero crossings distortions, low THD, high efficiency and low leakage current. The analytical and simulation results showed that this topology has an efficiency of 94.14%, a THD of 2.62% and a leakage current of 22.10mA. For the HERIC topology, the efficiency and THD are 94.13% and 3.26%, respectively.

From power quality point of view and based on the analysis presented in Section III, it is anticipated that the low frequency harmonics are significantly reduced as shown in Fig. 7.

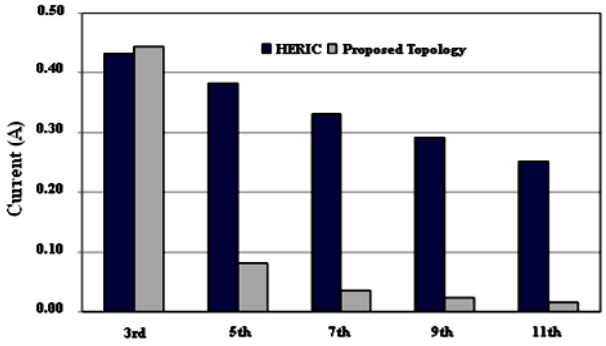

Fig.7. Comparison of low order harmonics in the HERIC and proposed topologies.

It is obvious that, for the proposed topology, low order harmonics are much less than those of the HERIC topology. This represents another advantage for the proposed topology.

Table 3. Losses Breakdown for the HERIC and the Proposed Topologies

	HERIC	Proposed
Conduction losses (W)	295.75	220.30
Switching losses (μW)	112.80	111.00
Diodes losses (W)	0.00	74.77
Total losses (W)	297.55	295.07
Input power (W)	5034.00	5034.00
Efficiency (%)	94.09	94.14

7. Conclusion

In this paper, major transformerless topologies were reviewed in terms of their advantages and disadvantages. It was found that these topologies suffer from some drawbacks such as the leakage current and zero crossings distortions. The leakage current is generated when the transformer is omitted. However, the zero crossings distortions are due to the applied control strategies. Accordingly, a novel transformerless inverter topology was developed and a detailed analysis of its efficiency was carried out. It was found that the adopted topology as well as the control strategy has revealed that the zero crossings distortion was definitely eliminated, the efficiency has been improved and the low frequency harmonics were significantly reduced.

Following these preliminary results, a prototype is under design to confirm experimentally the above mentioned features of the proposed topology.

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