Implementation and Performance Analysis of a Single Phase Synchronization Technique based on T/4 Delay PLL

Iwan Setiawan*‡, Trias Andromeda*, Mochammad Facta*, Hermawan*, Susatyo Handoko*

*Department of Electrical Engineering, Universitas Diponegoro (Undip), Semarang 50275 Indonesia.

(iwansetiawan@live.undip.ac.id, trias1972@gmail.com, mochfacta@gmail.com, hermawan.60@gmail.com, susatyo73@gmail.com)

‡ Corresponding Author: Iwan Setiawan, Kampus Teknik Elektro Undip Tembalang Semarang, Indonesia, Tel: +62 24 7460057, Fax: +62 24 7460057, iwansetiawan@live.undip.ac.id

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Abstract- The proper operation of current controllers in the grid tie inverter systems strongly depend on the accuracy of grid phase detection algorithm of the phase locked loop. The main aim of this paper is besides to implement a single phase synchronization technique base on T/4 delay PLL, also to investigate the effect of the PLL control bias to the PLL ouput performance mainly in the steady state conditions. To optimize execution time of the PLL, in this work, the real time T/4 delay PLL software algorithm is realized by using fixed point arithmetic computation technique that embedded in the 16 bit-wide digital signal controller dsPIC30f4011. Based on the experimental results, the accurate phase detection of the PLL in the steady state basicaly could be achieved by utilizing a relatively high control bias even with just using a simple proportional controller. Whereas, for a relatively low control bias, the accurate phase detection of the PLL just could be achieved by utilizing a proportional integral controller.

Keywords current controller, grid-tie inverter, T/4 delay PLL, fixed point arithmetic.

1. Introduction

In recent years, three phase grid-connected inverters play important role in power application, they could be found in HVDC systems [1], STATCOM [2], DFIG-based wind turbines [3][4], large scale PV system [5][6] and active rectifiers. Not only for three phase system, nowandays, grid connected inverters could also be found in single phase systems. In these systems, the grid-connected inverters could be found mainly in small scale on-grid renewable power generation systems, such as on-grid PV systems[7][8][9].

For the proper operation of the grid- tie inverter systems, the information of the fundamental grid voltage phase which estimated by a phase locked loop (PLL) algorithm should be accurate. In grid tie inverter systems, the grid voltage phase is needed by the inverter control system to synchronize output current with the grid voltage such that active and reactive power injected to the grid could be controlled [10][11].

Based on its structure, there are several popular single phase PLLs reported by literatures, such as invers park transform based PLL, Second order generilzed integrator (SOGI) based PLL, Hilbert Transform based PLL, T/4 delay PLL, and Enhanced PLL [12-16]. In general, the major difference among the PLL topologies is the way how the orthogonal signal of the input is generated by the orthogonal signal generator (OSG) [17].

Each of the PLL basically have their own advantages and drawbacks. Due to simplicity in the structure and low computation requirement, among the single phase PLL techniques, the T/4 delay based PLL is a good choice for implementation, mainly in restricted resource microcontroller such as 16 bit wide digital signal controller.

The main aims of this paper are: (1) To design and realize T/4 delay based PLL in the low cost-high performance 16 bit wide dsPIC30F4011 digital signal controller, (2) to analize the influence of the bias control of the PLL to output performance.

To get the optimum execution rate, in this work, the PLL algorithm is implemented by using fixed point arithmetic computation, whereas the sinusoidal of the grid phase is precalculated and stored in 8 bit width array.

The remainder of the paper is organized as follows. Section 2 describes the 4/T delay based PLL topology. Section 3, present a step by step design and implementation of the PLL algorithm in dsPIC DSC platform. Next, Section 4 present the experimental results and discuss the steady state performance of the PLL feedback system. Finally, the conclusions are drawn at Section 5.

2. Model of a T/4 Delay Based PLL

Phase locked loop basically is a feedback control system which control the phase of a locally generated signal to track the phase of the PLL signal input. In grid tie inverter systems, the main purpose of a PLL is to synchronize the phase of the inverter current output to the phase of the grid voltage, so that the active and reactive power injected to the grid could be control independently. Besides grid phase information, the PLL could also used to monitor grid voltage magnitude and the grid frequency for performance monitoring purposes.

Fig.1 shows a general topology of the single phase PLL based on a T/4 delay orthogonal signal generator (OSG). As shown in Fig. 1, In the T/4 delay based PLL, the quadrature signal input simply generated by delaying the input signal with amount ¼ periode. These time varying signal then transform to dc form by mean of park trasform (eq. 1) where the phase information fed to the park transformation block is derived from the output of the PLL feedback system .

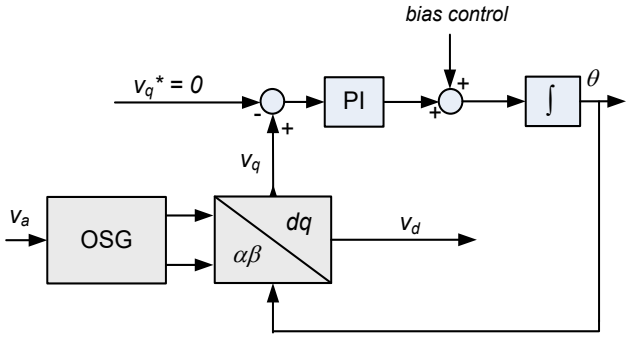


Fig.1. Single phase PLL based on orthogonal signal generator

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \quad (1)$$

The principal operation of the grid voltage synchronization of the PLL feedback system itself basically could be explained by refer to Fig.2. As shown at the Fig.2, the objective of the PLL feedback control system is to bring the quadrature signal (v_q) to zero value such that the output phase of the PLL will match the input grid voltage phase.

If the PLL control bias is set close to the nominal grid voltage frequency such that the phase error is relatively small, then the open loop and the closed loop transfer function of the PLL plant mathematically could be model as shown at (2) and (3) respectively:

$$H(s) = \frac{1}{s} \quad (2)$$

$$H(s) = \frac{d(s)}{s+d(s)} \quad (3)$$

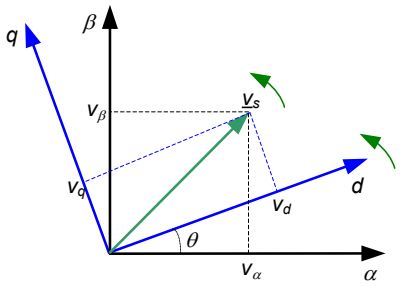


Fig.2. Grid voltage synchronization process of the PLL

3. Hardware Setup and Software Design of The T/4 Delay Single Phase PLL

3.1. Hardware Setup

Fig. 3 and 4 respectivelly show the hardware block diagram and hardware setup of the designed PLL. In this work, the PLL algorithm is embedded into a 16 bit wide digital signal controller dsPIC30f4011 producted by Microchip. The grid voltage in which its phase will be detected is read by internal ADC via voltage sensor ZMPT101B that available commercially.

Due to dsPIC30f4011 have no internal DACs, then to monitor internal variables in the program, such as the real grid voltage, phase and grid voltage estimation resulted by the PLL, a dual channel 8 bit DAC AD7302 is utilized in this work.

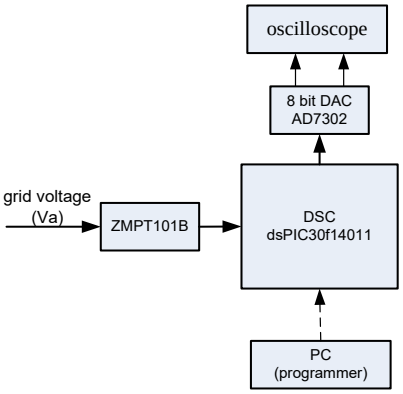


Fig.3. Hardware block diagram

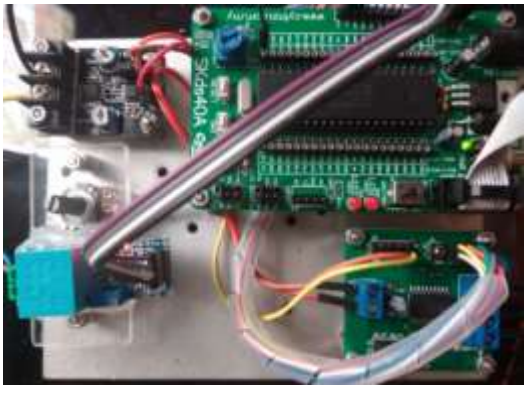


Fig.4. Hardware Setup

3.2. Software Design and Implementation

By refer to eq. (3), then the closed loop transfer function for proportional and proportional-integral controllers each could be represented respectivelly by (4) and (5):

$$H_{cl}(s) = \frac{K_p}{s+K_p} \quad (4)$$

$$H_{cl}(s) = \frac{K_p s+K_i}{s^2+K_p s+K_i} \quad (5)$$

By using final value theorm of Laplace transformation, it could be proved that both of the transfer functions above will be stable and have zerro steady state error for positive proportional and integral gains which is chosen.

In this work, the grid voltage input signal and the T/4 delay PLL algorithm are sampled and executed every 0.1 ms (execution rate = 10 Khz).

By considering the nominal frequency of the grid voltage is about 50 Hz, then for 10 kHz execution rate, the quadrature signal of the grid voltage input is derived simply by delaying *50* sample of the input signal.

To get fast real time execution time, in this work, the sinusoidal wave values that need by Park transform block have been precalculated and stored in 8 bit wide table, whereas the PLL algorithm is implemented by using fixed point arithmetic computation technique, where all of the internal variable are declared by using signed and unsigned integer data type and represented by per-unit (PU).

Fig. 5 and Table 1 below respectively show designed software dataflow model of the T/4 based PLL and their internal variables that used in the real time software.

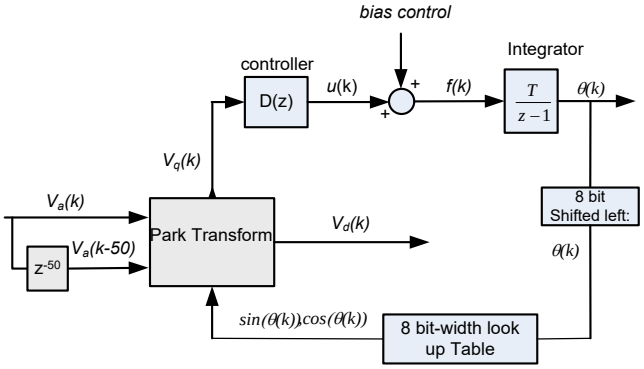


Fig.5. Software dataflow diagram of the designed PLL

Table 1. Internal variables that used in the real time software

Internal program variable	Data type	Range in PU
Grid voltage input signal	signed integer	[-1:1]
T/4 delayed voltage input signal	signed integer	[-1:1]
Direct axis signal	signed integer	[-1:1]
quadrature axis signal	signed integer	[-1:1]
Output controller	signed integer	[-1:1]
Frequency	unsigned integer	[0:1]
Phase angle	unsigned char	[0:1]
Sin(.)	signed integer	[-1:1]
Cos(.))	signed integer	[-1:1]

For the implemented software, the grid voltage magnitude and the grid frequency which are could be detected respectively are in the range [0: 340] volt and [0-52] Hz, so the base of the grid voltage magnitude and the frequency each are 340 volt and 52 Hz.

4. Experimental Results and Discussion

In this section, all results obtained during the experiment will be presented and analized. Due to one of the main objective of this work is to investigate the effect of the control bias to the PLL output accuracy, in this experiment we use two relatively different control bias: (1) a relatively low control bias: 42 Hz (0.807 pu) and (2) a relatively high control bias: 49 Hz (0.94 pu).

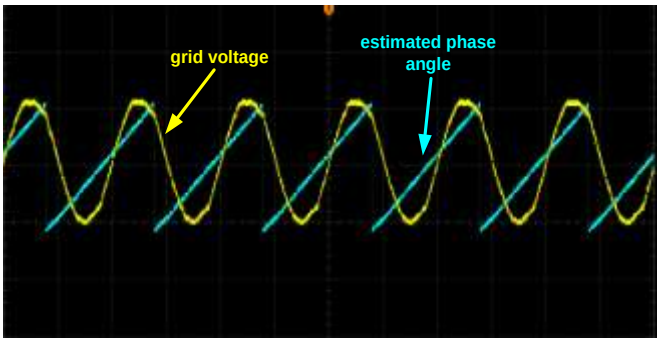
For the each control bias used in the software, we investigate the PLL output perfomance for two different clasical controllers : a proportional controller and a Proportional-Integral controller.

4.1. PLL output performance with a relatively low control bias

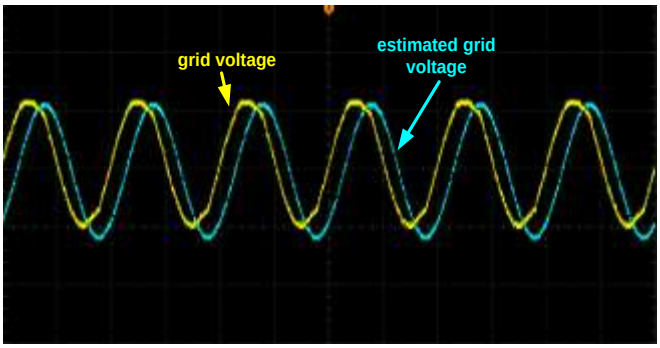
a. Proportional Controller

For the relatively low control bias (0.807 pu), the phase output and the estimated grid voltage of the PLL for the proportional controll scheme are depicted at Fig. 6 and 7.

Fig. 6(a) show the plots of the grid voltage (yelow) and its phase angle which is estimated by the PLL (light blue) based on proportional controll scheme with the relative low proportional gain 0.5.



(a)



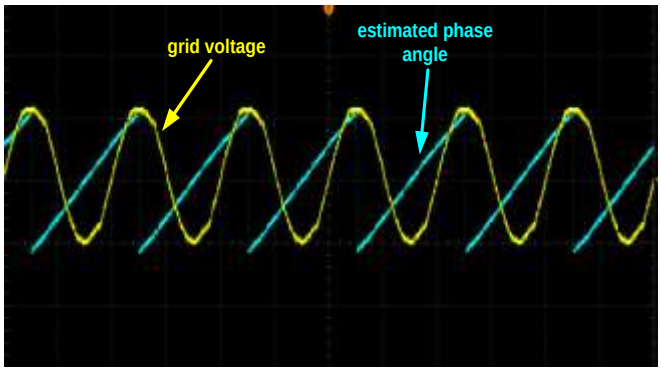
(b)

Fig.6. Outputs of the PLL based on proportional controller with K_p = 0.5 (yellow: grid voltage, blue: esimated phase (a) and estimated grid voltage (b))

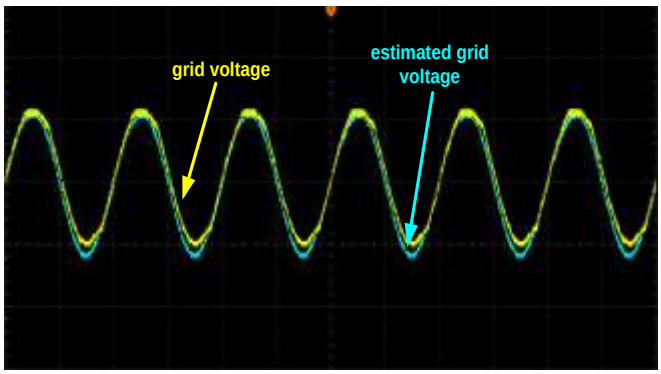
Based on Fig. 6(a) and 6(b), ones can see that the grid voltage phase angle estimated by the PLL for the relative low proportional gain although stable in steady state condition, however it is not acurrate. In this case, the estimated voltage phase is laging about 45^o from the true phase.

For the low control bias, the accuracy of the phase estimation of the PLL practically cauld be improved by increasing the proportional gain of the controller.

Fig. 7(a) and 7(b) show the plots of the estimation phase and grid voltage (light blue) from the PLL along with the true grid voltage (yelow) based on a relatively high gain proportional control scheme, ones can see that the estimation of the phase angle error at steady state in Fig. 7 is about zero.



(a)



(b)

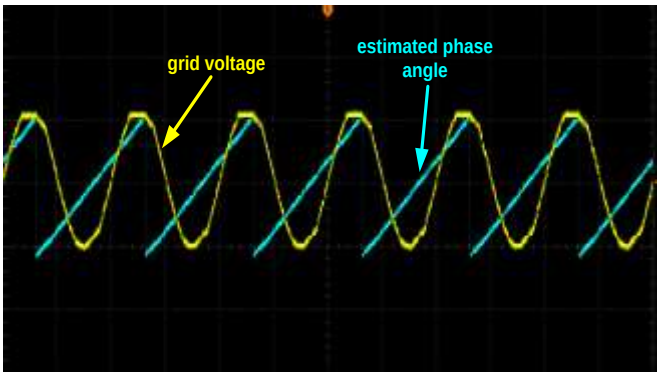
Fig.7. Outputs of the PLL based on proportional controller with K_p = 0.9 (yellow: grid voltage, blue: esimated phase (a) and estimated grid voltage (b))

b. *Proportional Integral Controller*

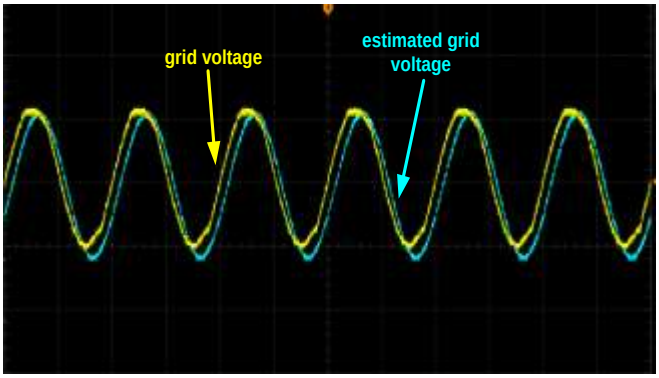
Fig. 8 and 9 respectively show the outputs of the PLL based on proportional - integral controll scheme with the same integral gain (K_i = 0.3) but with diferrent proportional gains: 0.5 and 0.9.

As shown from the plots of Fig. 8, For relatively lower proportional gain, although there is still steady state phase error about 15^o, however by using integrator component, this error relatively lower compared with Fig 6.

Once again, as shown at Fig. 9, the accuracy of the phase estimation of the PLL cauld be improved by increasing the proportional gain of the controller. From the plots, ones could see that the steady state error of the phase estimation is about zero.

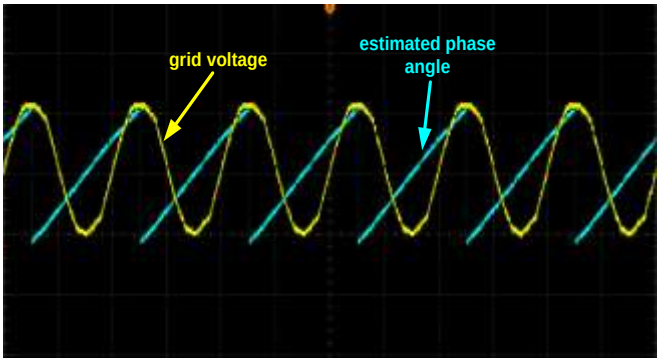


(a)

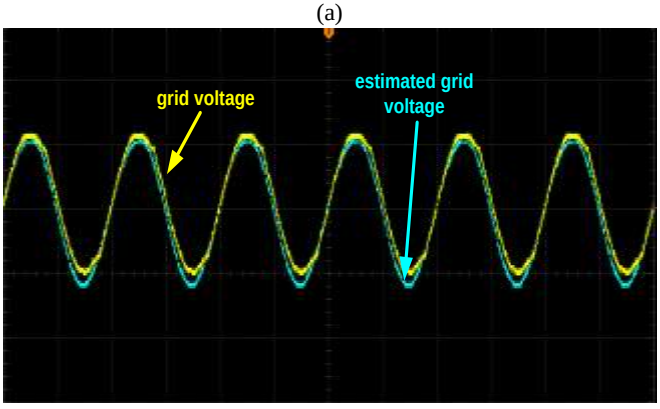


(b)

Fig.8. 0utputs of the PLL based on proportional-integral controller with K_p = 0.5 and K_i = 0.3 (yellow: grid voltage, blue: esimated phase (a) and estimated grid voltage (b))



(a)



(b)

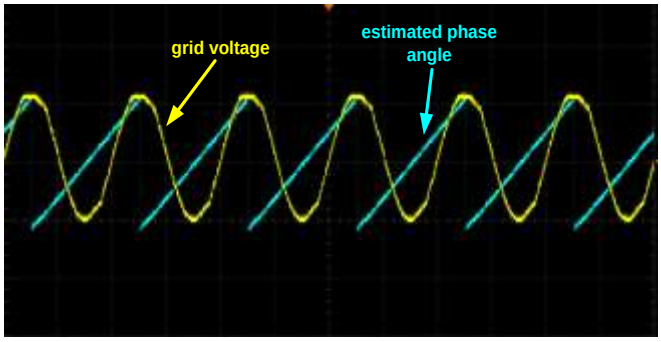
Fig.9. Outputs of the PLL based on proportional-integral controller with K_p = 0.9 and K_i = 0.3 (yellow: grid voltage, blue: esimated phase (a) and estimated grid voltage (b))

4.2. PLL output performance with a relatively high control bias

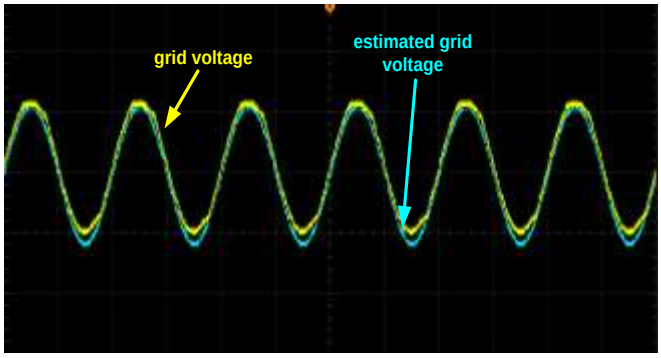
a. Proportional Controller

For the relatively high control bias (0.94 pu), the phase output and the estimated grid voltage of the PLL for the proportional controll scheme could be seen at the plots in Fig. 10 (for a relatively low gain proportional : 0.5) and 11 (for a relatively high gain proportional : 0.9)

As shown at Fig. 10 and 11, the result of the grid phase estimation in steady state condition for the relatively high control bias is relatively accurate, with error is a almost zero although the utilized feedback controller is just a proportional control system.



(a)



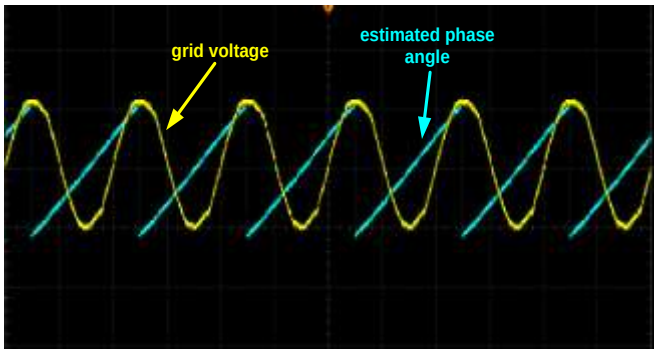
(b)

Fig.10. Outputs of the PLL based on proportional controller with K_p = 0.5 (yellow: grid voltage, blue: esimated phase (a) and estimated grid voltage (b))

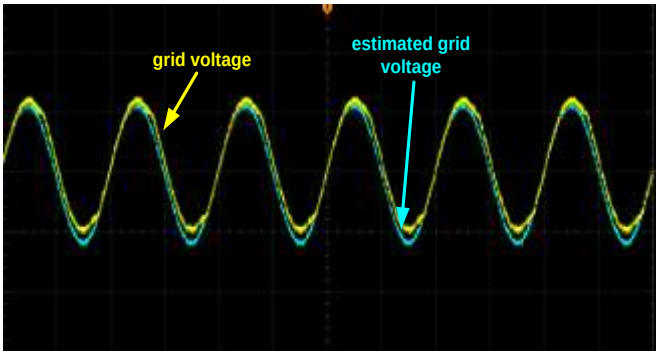
b. *Proportional Integral Controller*

Fig. 12 and 13 respectively show the phase output and the grid voltage estimation of the PLL based on proportional - Integral controll scheme with the same integral gain (K_i=0.3) but diferrent proportional gain : 0.5 and 0.9.

As depicted at Fig. 12 and 13, in the steady state condition, the estimation result of the PLL with the high control bias are relatively accurate with almost zero error both for low or high gain proportional. Also, ones can see that compared to Fig 10 and 11, in the steady state the utilizing of the proportional-integral controller compared to proportional controller practically will not improve the accuracy of the phase estimation.

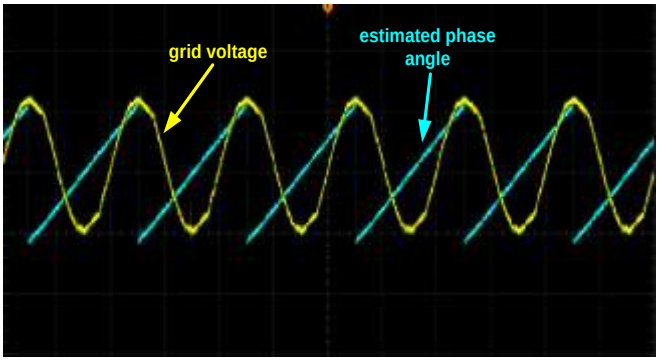


(a)

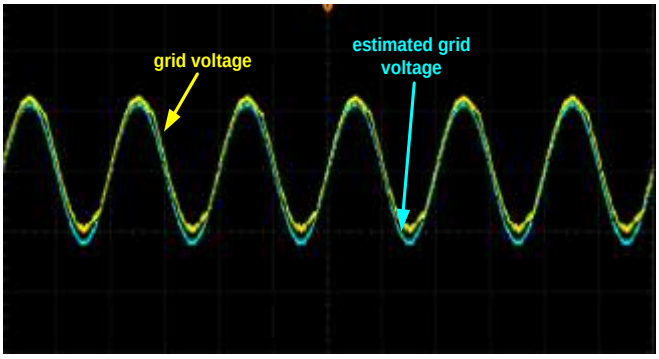


(b)

Fig.11. Outputs of the PLL based on proportional controller with K_p = 0.5 (yellow: grid voltage, blue: esimated phase (a) and estimated grid voltage (b))

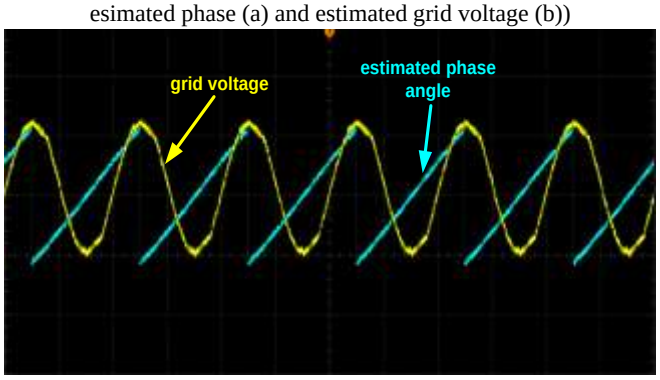


(a)

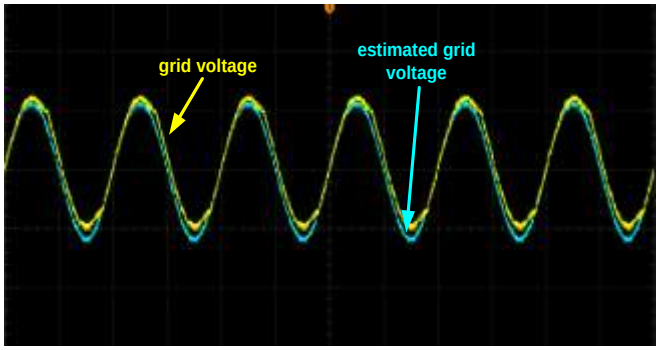


(b)

Fig.12. Outputs of the PLL based on proportional-integral controller with K_p = 0.5 and K_i = 0.3 (yellow: grid voltage, blue: esimated phase (a) and estimated grid voltage (b))



(a)



(b)

Fig.13. Outputs of the PLL based on proportional-integral controller with K_p = 0.9 and K_i = 0.3 (yellow: grid voltage, blue: esimated phase (a) and estimated grid voltage (b))

5. Conclusion

The investigation of the effect of the control bias in the single phase T/4 delay based PLL to the accuracy of the grid voltage phase estimation in the steady state have been conducted in this works. Based on real time implementation, it is shown that the steady state performance of the single phase PLL strongly depend on the control bias magnitude. For the relatively high control bias, the very simple proportional feedback controller practically could be estimate grid voltage phase accurately, whereas for the relatively low control bias magnitude, the high performance of the PLL outputs just could be derived by a proportional-integral control scheme.

Acknowledgements

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